REMARKS

Present Status of the Application

The Office Action rejected claims 1-13. Specifically, the Office Action rejected claims 1, 2, 4, 5, 7-9, 11, and 12 under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al., (U. S. Patent 6,340,961; hereinafter Tanaka) in view of Nagaoka et al. (U. S. Patent 5,943,032; hereinafter Nagaoka). In addition, the Office Action rejected claims 3, 6, 10, and 13 under 35 U.S.C. 103(a) as being unpatentable over Tanaka (U. S. Patent 6,340,961) in view of Nagaoka and further in view of Grossman et al. (hereinafter Grossman). The Office action also objected claims 3, 6, 10, and 13. Applicants have amended claims 3, 6, 10, and 13 to overcome objections. After entry of the foregoing amendments, claims 1-13 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Claim Rejections under 35 USC 103

The Office Action rejected claims 1, 2, 4, 5, 7-9, 11, and 12 under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Nagaoka. In addition, the Office Action rejected claims 3, 6, 10, and 13 under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Nagaoka and further in view of Grossman. Applicants respectfully traverse the rejections for at least the reasons set forth below.

1. With respect to **independent claims 1, 8, and 11**, as for example shown in FIG. 3, the

recited features includes

the error diffusion unit 320, coupled to the inverse γ conversion lookup unit to receive the first gray scale data, and to ***modify the first gray scale data into a second gray scale data recorded as a display brightness error of the currently displaying pixel by considering a display brightness error of a neighboring pixel of the currently displaying pixel***.

In re Tanaka, the Office Action has referred to [data correcting circuit 35] of Tanaka as the error diffusion unit of the present invention. However, Applicants respectively disagree.

Tanaka discloses the data correcting circuit 35 as follows (FIG. 4; col. 7, line 56 – col. 8, line 19):

> *"The data correcting circuit 35 has a frame memory 36 inserted in one of two signal lines from the gamma corrector 33. The two signal lines from the gamma corrector 33 are connected to a processing circuit 37 of the data correcting circuit 35.*
>
> *The signal input units 34a-34c are connected to a pattern generator 38 of the data correcting circuit 35. The pattern generator 38 is connected to the processing circuit 37.*
>
> *The signal input unit 34b is connected to a dot clock generator 39 which is connected to the pattern generator 38.*
>
> *The frame memory 36 temporarily stores one frame, at a time, of gradation data and outputs the stored frame after having delayed same for a period of time which corresponds to the duration of one frame.*

The processing circuit 37 has a LUT (Look-Up Table) 40 which stores corrective data that can be addressed by gradation data of a preceding frame and gradation data of a present frame. The processing circuit 37 also has a data reading circuit 49 and a correction executing circuit 50. The data reading circuit 49 reads corrective data from the LUT 40 which have been addressed by gradation data of a present frame directly supplied from the gamma corrector 33 and gradation data temporarily stored in the frame memory 36.

Since gradation data comprise numerical values representing gradation levels, for example, the corrective data are established as numerical values for increasing and reducing the numerical values representing gradation levels.

The correction executing circuit 50 adds positive or negative numerical values of the corrective data read from the LUT 40 to the numerical values representing gradation levels of the gradation data of the present frame, for thereby correcting the gradation data with the corrective data. (emphasis added)".

As also referring to Fig. 4 of Tanaka, the Gamma signals are divided into two paths in the data correcting circuit 35, in which one path goes through the frame memory 35. Then, two paths are fed to the processing circuit 37. The processing circuit 37 includes the look-up-table 40 with the data reading circuit 49 and the correction executing circuit 50. *The data reading circuit 49 reads corrective data from the LUT 40 which have been addressed by gradation data of a present frame directly supplied from the gamma corrector 33. The correction executing circuit 50 adds positive or negative numerical values of the corrective data read from the LUT 40 to the numerical values representing gradation levels of the gradation data of the present frame.*

Clearly, Tanaka in above disclosure does not equally disclose the operation mechanism as recited in independent claims, as emphasized above.

Further still, in the present invention, the recited gray scale lookup unit 330 receives the output from the error diffusion unit 320 to obtain a sustain pulse number by a look-up table.

However, the drive circuit 3 in Fig. 4 of Tanaka is a usual driver bit not the look-up table. More specifically, the sustain driver 62 is driven by the drive circuit 3. Tanaka does not disclose the features of the recited gray scale lookup unit 330 of the present invention, when considering the circuit as a whole.

In re Nagaoka, Nagaoka (col. 2, lines 15-19) states:

> *An object of the present invention is to provide a gray scale controlling method for a plasma display device which enhances the display quality of the plasma display device by establishing a linear relation between the gray level and the corresponding brightness.*

However, this at least does disclose "*...a second gray scale data recorded as a display brightness error of the currently displaying pixel...*" as recited in independent claims.

Nagaoka still does not supply the missing features in Tanaka as discussed above.

For at least the fore going reasons, the independent claims 1, 8, and 11 are distinguishable over the prior art references.

2. With respect to claim 2 and 5, the ***error diffusion unit*** in FIGs. 3-5 is recited in more detail. Particularly, the weighted error supply circuit 323 weights the output from the

brightness error lookup circuit 322 by for example a, b, c, d, and the adder 321 adds the weighted error information, so as to produce an output to the gray scale lookup unit 330.

The LUT of Tanaka does not specifically disclose the same circuit structure as recited in claim 2 and 3.

Therefore, claims 2 and 5 are distinguishable over the prior art.

3. With respect to dependent claims 4, 7, 9, and 12, according to at least the same foregoing reasons applied to independent claims 1, 8, 11 and dependent claims 2 and 5, claims 4, 7, 9, and 12 are distinguishable over the prior art.

4. With respect to claims 3, 6, 10, and 13, for at least the same foregoing reasons, claims 3, 6, 10, and 13 are distinguishable over the prior art.

More specifically in addition, Nagaoka (col. 9, lines 31-51; col. 10, lines 1-29; Gig. 7) failed specifically define the error function by "$E=[(B(G)-B(G_0))/B_0(G)]*G$" in the specific consideration of the present invention. Please note that the "$[(B(G)-B(G_0))/B_0(G)]$" is timed with "G" again, *associating with the weighted error supply circuit*, for this specific correction on the gray scale in the present invention.

In re Grossman, again, the specific error function as recited in claims 3, 6, 10, and 13 is not specifically disclosed. Grossman only discloses the percent error but does not disclose the specific error function, associating with the *weighted error supply circuit* in the invention, when

considering the invention as a whole.

For at least the foregoing reasons, Applicants respectfully submit that independent claims 1, 8, and 11 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-7, 9-10, and 12-13 patently define over the prior art references as well, wherein claims also mores specifically distinguish over the prior art references.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-13 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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